What is claimed is;

1. A semiconductor device comprising:

a semiconductor chips,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to said stress relaxing layer of said semiconductor chip.

2. A semiconductor device comprising:

a semiconductor chips,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to said stress relaxing layer of said semiconductor chip, and

respective side planes of said stress relaxing layer,

said semiconductor chip, and said organic protecting film are exposed outside on a same plane.

3. A semiconductor device comprising:

a semiconductor chips,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

via-holes provided between the electrodes on said semiconductor chip and said circuit layer,

conductive portions for connecting electrically said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern,

an organic protecting film provided on the plane opposite to the plane where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside on a same plane.

4. A semiconductor device as claimed in any one of ~~claims from~~ claim 1 to claim 3, wherein

said organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of said stress relaxing layer.

5. A semiconductor device as claimed in claim 3, wherein said stress relaxing layer is composed of porous polytetrafluoroethylene.

6. A semiconductor device as claimed in claim 3, wherein said conductive portion in said via-hole is composed of conductive resin.

7. A semiconductor device as claimed in claim 3, wherein said conductive portion in said via-hole is composed of conductor formed by plating.

8. A semiconductor device as claimed in claim 3, wherein said conductive portion in said via-hole is composed of conductor formed by vapor deposition.

9. A semiconductor device comprising:

semiconductor chips,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically said circuit layer and said electrodes on said semiconductor chip,

external terminals provided at designated portions on said circuits in a grid array pattern,

an organic protecting film provided on the plane

opposite to the plane, where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside on a same plane.

10. A semiconductor wafer comprising:

plurality of chip areas comprising circuits and electrodes, respectively,

a stress relaxing layer provided on a plane, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer, and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to the plane, whereon said stress relaxing layer is provided, of said chip areas.

11. A semiconductor wafer comprising:

plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

via-holes provided between said electrodes and said

circuit layer,

conductive portions for connecting electrically said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the stress relaxing layer of said chip area.

12. A semiconductor wafer as claimed in any one of claims 10 and 11, wherein

said organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of said stress relaxing layer.

13. A semiconductor wafer as claimed in any one of claims 10 and 11, wherein

said stress relaxing layer is composed of porous polytetrafluoroethylene.

14. A semiconductor wafer as claimed in claim 11, wherein

said conductive portion in said via-hole is composed of conductive resin.

15. A semiconductor wafer as claimed in claim 11, wherein

said conductive portion in said via-hole is composed of conductor formed by plating.

16. A semiconductor wafer as claimed in claim 11, wherein

said conductive portion in said via-hole is composed of conductor formed by vapor deposition.

17. A semiconductor wafer comprising:

plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically said electrodes on said chip area and said circuit layer,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, wherein said circuits and electrodes are formed, of said chip area.

18. A method for manufacturing semiconductor device comprising the steps of:

forming a stress relaxing layer on a plane, whereon circuits and electrodes of respective chip areas are formed, of a semiconductor wafer,

forming an organic protecting film on the plane opposite to the plane, where the electrodes of said respective chip areas,

forming via-holes in said stress relaxing layer on said

chip areas,

forming conductive portions in said via-holes,

forming circuits on said stress relaxing layer,

forming external terminals on said circuit layer, and

cutting said chip areas, the substrate comprising said circuits, and said organic protecting film along a same plane so that the semiconductor device obtained by the cutting becomes a minimum operation unit.

19. A method ~~for~~ manufacturing semiconductor device comprising the steps of:

forming circuit layer on a porous stress relaxing layer,

adhering said stress relaxing layer comprising the circuit layer to a plane, whereon electrodes are formed, of a chip area,

forming an organic protecting film ~~to~~ on a plane opposite to the plane comprising said chip area,

forming via-holes in said stress relaxing layer,

forming a conductive portions in said via-hole,

forming external terminals on said circuit layer, and

cutting said chip areas, the substrate comprising said circuits, and said organic protecting film along a same plane so that ~~the~~ semiconductor device obtained by the cutting becomes a minimum operation unit.

20. A semiconductor module mounted with plurality of semiconductor devices as claimed in any one of claims ~~from~~

1 to 9.